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SYSTEM AND METHOD OF MEASURING TURN-ON AND TURN-OFF TIMES OF AN OPTOELECTRONIC DEVICE

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A SYSTEM AND METHOD OF MEASURING TURN-ON AND TURN-OFF TIMES OF AN OPTOELECTRONIC DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[001] This application claims the benefit of U. S. Provisional Application No. 60/422,598, filed October 31, 2002.

BACKGROUND OF THE INVENTION

The Field of the Invention

[002] The present invention relates generally to optical devices in high-speed communication networks. More particularly, the present invention relates to systems and methods for measuring the turn-on and turn-off times of optical circuitry in an optoelectronic device.

The Related Technology

[003] Devices such as optoelectronic transceivers include lasers and electronic elements that must be turned on and off rapidly in order to, for example, be used effectively in passive optical networks. Passive optical networks are described in Applicant's United States Provisional Patent Application Serial No. 10/188,575, filed September 5, 2002 and entitled "SYSTEM FOR CONTROLLING BIAS CURRENT IN LASER DIODES WITH IMPROVED SWITCHING RATES," which is incorporated herein by reference.

[004] Passive optical networks enable optoelectronic transceivers to share optical fibers while transmitting and receiving data in an optical form. Generally, a transceiver may not use all the bandwidth available on a fiber because data transmission is

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intermittent. As a result, transmitting and receiving data on optical fibers using more than one optoelectronic transceiver helps maximize the use of the network's bandwidth.

[005] A passive network system utilizes the bandwidth available on a fiber by turning on a second transceiver when the first transceiver stops transmitting. Likewise, when the second transmitter finishes transmitting, another transmitter transmits data and so forth. Typically, passive optical networks employ a time division multiplexing access (TDMA) scheme to make this possible. In such schemes, the data transmission capabilities of the optoelectronic transceivers are operational only during separate, non-overlapping periods of time. Overlapping transceiver signals can cause unacceptable transmission errors in the passive optical network.

[006] Because transceivers cannot transmit overlapping data, it is useful to ensure that a particular transceiver is completely off before the next transceiver begins transmitting data. However, when an optoelectronic transceiver receives a command to disable its optical transmitter circuitry, the response is not instantaneous. Instead, a measurable amount of time passes before the command is effectuated and the optical transmitter circuitry is turned off. Similarly, when an optoelectronic transceiver receives a command to enable its optical transmitter circuitry, the response time is also measurable. The amount of time required for turning optical transmitter circuitry on and off determines when a subsequent transmitter should be enabled to transmit data without causing an overlap in transmission with the first transceiver.

[007] One method for ensuring that data does not overlap is to wait a predetermined period of time that is long enough to ensure that the first transceiver is not transmitting data when the subsequent transceiver begins transmitting data. However, this approach will likely result in unnecessarily long periods of time where

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the network is not transmitting data while it waits to ensure that the first transceiver has stopped. This approach fails to accomplish the object of utilizing as much of the network's bandwidth as possible.

[008] Transceivers can make better use of network bandwidth by causing the subsequent transceiver to begin data transmission as soon as possible following the termination of data transmission by the first transmitter. Knowing the delay time for turning the transceiver on and off is useful for determining when a transceiver can be enabled without causing overlap in data transmission. By accounting for delay in the transceiver's turn-on and turn-off time, the transceiver can be configured to transmit data with much less delay between multiple transceiver transmissions than would otherwise be possible.

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BRIEF SUMMARY OF THE INVENTION

[009] The present invention relates to systems and methods for measuring the time required for an optoelectronic device to turn on and/or off. Embodiments of the invention are useful for optimizing the use of bandwidth in a passive optical network. By measuring the time needed to turn an optoelectronic device on or off, the bandwidth of a single transmission line can be used more effectively.

[010] The systems and methods of the present invention measure the transceiver's turn-on and turn-off time. Passive optical networks use the delay time of the present invention to turn the multiple transceivers on and off such that no overlap will occur in data transmission and the time between successive transmissions will be minimized. By measuring the delay needed to turn a particular transceiver on or off, the command given to the next transceiver can be given such that the next transceiver begins transmitting after the turn-off time of the previous transceiver ends. In other words, the turn-off time for a particular receiver overlaps with the turn-on time of the next transceiver to minimize the delay between successive transceivers.

[011] In one embodiment, the method for determining a turn off time includes the steps of 1) generating a first bit sequence by reference to a controlling pattern; 2) transmitting the first bit sequence to an optoelectronic device; 3) receiving the first bit sequence from the optoelectronic device and a second bit sequence generated by reference to the same controlling pattern; 4) commanding the disablement of the optoelectronic device after initiating the generating step; 5) comparing bit groups from the first bit sequence received from the optoelectronic device to corresponding bit groups in the second bit sequence - this step begins when the commanding step is executed; 6) maintaining a count that is incremented each time the comparing step is

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executed; 7) storing each bit group from the first bit sequence received from the optoelectronic device that does not match a corresponding bit group in the second bit sequence along with a corresponding value of the count; 8) terminating the comparing step when a bit group from the first bit sequence received from the optoelectronic device indicates that the optoelectronic device is turned off; and 9) computing the turn-off time by reference to one or more of the stored bit groups and corresponding counts.

[012] The present invention also includes a method for measuring a turn-on time of an optoelectronic device. The method includes the steps of 1) generating a first bit sequence by reference to a controlling pattern; 2) transmitting the first bit sequence to an optoelectronic device; 3) receiving an output value of the optoelectronic device and a second bit sequence generated by reference to the controlling pattern - the output value corresponding to the first bit sequence when the optoelectronic device is enabled; 4) commanding the enablement of the optoelectronic device after initiating the generating step; 5) comparing groups of output values of the optoelectronic device to corresponding bit groups in the second bit sequence - this step beginning when the commanding step is executed; 6) maintaining a count that is incremented each time the comparing step is executed; 7) storing comparison results for each group of output values with an output value that matches a corresponding bit in a bit group in the second bit sequence along with a corresponding value of the count; 8) terminating the comparing step when an entire group of output values matches a corresponding bit group in the second bit sequence; and 9) computing the turn-on time by reference to one or more of the stored comparison results and corresponding counts.

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[013] These and other advantages and features of the present invention will become more fully apparent from the following description and appended claims, or may be learned by the practice of the invention as set forth hereinafter.

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BRIEF DESCRIPTION OF THE DRAWINGS

[014] To further clarify the above and other advantages and features of the present invention, a more particular description of the invention will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. It is appreciated that these drawings depict only typical embodiments of the invention and are therefore not to be considered limiting of its scope. The invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

[015] Figure 1 is a block diagram of a system consistent with an embodiment of the present invention.

[016] Figure 2 is a block diagram of a computer consistent with an embodiment of the present invention.

[017] Figures 3A-3E illustrate processing steps consistent with an embodiment of the present invention.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[018] Reference will now be made to the drawings to describe various aspects of exemplary embodiments of the invention. It is to be understood that the drawings are diagrammatic and schematic representations of such exemplary embodiments, and are not limiting of the present invention, nor are they necessarily drawn to scale. Moreover, while various headings are employed in the following discussion, such headings are included solely for the purpose of organizing and facilitating the disclosure hereof and are not intended, nor should they be construed, to define the invention or limit the scope of the invention in any way.

I. General Description of Aspects of An Exemplary Operational Setup

[019] Embodiments of the present invention are used in a passive optical network to enable a plurality of optoelectronic transceivers to share one or more optical fibers while transmitting and receiving data in an optical form. While some of the embodiments described herein refer to optical networks, it should be understood that the present invention can be employed in other types of networks.

[020] In one embodiment of a passive optical network, a plurality of optoelectronic transceivers are installed on a host device in the network. The transceivers are operably connected to one or more optical fibers such that multiple transceivers can transmit data on the same optical fiber. Consistent with network configurations, data transmitted over the optical fibers is then received by another set of transceivers that are connected with the network.

[021] Referring to Figure 1, there is shown a system 1 consistent with an embodiment of the present invention. As illustrated in Figure 1, the system 1 includes a circuit board 5, a first bit sequence ("BS") generator 10, a serializer/deserializer

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("SERDES") 20, a programmable delay 30, a deserializer 90, a second BS generator 100, a controller 130, a clock source 145, and a computer 160. Connected to the system 1, as illustrated in Figure 1, are a device under test ("DUT") 170 and a master device 180. In one embodiment of the invention, DUT 170 is an optical transceiver in a fiber optic network.

[022] The circuit board 5 is typically an insulated board that houses interconnected circuitry. The circuit board 5 typically provides power and ground connections (not illustrated) for various components mounted thereon.

[023] The BS generators illustrated in Figure 1 (*i.e.*, the first and second BS generators 10, 100) are typically one or more types of linear feedback shift registers. For example, a given BS generator may be a binary shift register with taps that are modulo-2 added together and fed back to the binary shift register as input. Persons skilled in the art recognize that the configuration and function of the taps, or similar circuitry, typically define bit sequences produced by a BS generator. In particular, these configurations and functionalities define a second bit group that is produced when a first bit group is input to a BS generator.

[024] The bit groups generated by a BS generator are typically output simultaneously in parallel form, but may be output serially as well. Additionally, bit sequences generated by a BS generator are preferably pseudo random bit sequences (or other deterministic sequences such as Gold, JPL, and Barker Codes). As a result, a plurality of BS generators can be configured in the same way so that each produces the same bit group from like input.

[025] The BS generators illustrated in Figure 1 preferably include an I/O port 12, a D_{in} port, a D_{out} port (*i.e.*, the I/O port 12, D_{in} port 14, and D_{out} port 16 and the I/O port

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102, D_{in} port 104, and D_{out} port 106 of the first and second BS generators 10 and 100, respectively), and a port for receiving a clock signal originating from the clock source 145 (connections not illustrated).

[026] The D_{in} port is typically a parallel port (n signals, channels, lines, etc.), but may be a serial port (1 signal, channel, line, etc.), that is used to receive data such as bit groups (*e.g.*, a seed value that identifies a starting bit group in a sequence of bits). And the D_{out} port is typically a parallel port, but may be a serial port, that is used to transmit bit groups.

[027] The I/O port may be a parallel or serial port that is used to receive control signals from the controller 130. These control signals may, for example, configure a BS generator (*e.g.*, configure the taps or similar circuitry that typically defines the type of bit sequences produced and the cycle length, uniformity, and independence of these bit sequences) and initiate and/or terminate the generation of a bit sequence by a BS generator.

[028] The SERDES 20 is typically a device, such as an ON Semiconductor® 8-Bit parallel to serial converter MC100EP446, for receiving data in parallel and transmitting this data serially. As illustrated in Figure 1, the SERDES 20 includes a D_{in} port 22 and a D_{out} port 24. The D_{in} port 22 is typically used to receive bit groups in parallel and the D_{out} port 24 is typically used to serially transmit bit groups received through the D_{in} port 22.

[029] The SERDES 20 may also include one or more ports (not illustrated) for exchanging control signals with the controller 130 and for receiving a clock signal originating from the clock source 145. These ports enable the controller 130 to, for example, control how the SERDES 20 receives, transforms, and transmits data. These

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ports may, furthermore, include a plurality of separate signals for address bits, an alarm interrupt, a chip select, a write input, a read input, a bus type select, a test input, and an address latch enable.

[030] The programmable delay 30 preferably comprises a programmable delay circuit (*e.g.*, an ON Semiconductor ECL Programmable Delay Chip MC100EPI95). A data signal applied to an input of the programmable delay 30 reappears at an output of the programmable delay 30, after a delay of a specified amount of time. Preferably, both leading and trailing edges of data signal pulses are delayed by the same amount of time, which is typically programmable by the controller 130 using either a serial or parallel data input.

[031] The programmable delay 30 preferably includes a D_{in} port 32, a D_{out} port 34, a I/O port 36, and a port for receiving a clock signal originating from the clock source 145 (connections not illustrated). The data signal generated by the master device 180 is transmitted to the programmable delay 30 through the D_{in} port 32. The data signal, after the specified delay, is then transmitted to the deserializer 90 through the D_{out}, port 34. The controller 130 sets the delay of the programmable delay 30 through the I/O port 36, which functions as a control port accessible to the controller 130.

[032] The deserializer 90 is typically a device, such as a MICREL 3.3V AnyRate MUX/DEMUX SY87724L, for receiving data in parallel and transmitting this data serially. As illustrated in Figure 1, the deserializer 90 preferably includes a D_{in} port 92 and a D_{out}, port 94. The D_{in} port 92 is typically used to receive bit groups serially and the D_{out}, port 94 is typically used to transmit these bit groups in parallel.

[033] The deserializer 90 may also include one or more ports (not illustrated) for exchanging control signals with the controller 130 and for receiving a clock signal

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originating from the clock source 145. These ports enable the controller 130 to, for example, control how the deserializer 90 receives, transforms, and transmits data.

[034] The controller 130 typically comprises a computer processor on a microchip (*e.g.*, a Motorola® 8-bitprocessor or other chip combining an 8-bit architecture with an array of field-programmable logic). The controller 130 directs the operation of circuitry on the circuit board (not all connections illustrated) and stores and manipulates data provided by this circuitry. The controller 130 completes these tasks, under the direction of the computer 160. In one embodiment of the present invention, the controller 130 may not have the capacity to perform measurements, which are described below, without the computer 160.

[035] The controller 130 preferably includes a first I/O port 131, a D_{out} port 132, a second I/O port 133, a third I/O port 134, a fourth I/O port 135, a first D_{in} port 136, a second D_{in} port 137, a fifth I/O port 139, a sixth I/O port 140, and a port for receiving a clock signal originating from the clock source 145 (connections not illustrated). The controller 130 may send and receive control signals, configuration data, etc. to some or all of the circuitry and/or devices illustrated in Figure 1 without departing from the scope of the present invention.

[036] In particular, the controller 130 may configure the BS generators and trigger or terminate the generation of bit sequences by the BS generators. The controller 130 preferably sends data to the first BS generator 10 through the D_{out}, port 132. This data is typically a seed value for the generation of a bit sequence, but may be other data as well. Additionally, the controller 130 transmits and receives control signals, configuration data, etc. to the second BS generator 100 through the second I/O port 133.

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[037] The controller 130 communicates with the computer 160 through the fourth I/O port 135. In preferred embodiments, the computer 160 exchanges control signals and/or data with the controller 130, which interacts with some or all of the other circuitry on the circuit board 5, to setup, initiate, and monitor measurements of the DUT 170.

[038] The controller 130 also preferably includes logic for comparing a first group of bits to a second group of bits. More specifically, the controller 130 compares bits of like position within their respective group of bits (*e.g.*, the second bit in a first group of bits is compared to the second bit in a second group of bits). In addition to making such comparisons, the comparator preferably stores comparison results, which may include a specification of individual bits within a group of bits that do not match. The controller 130 preferably includes the D_{in} ports 136, 137 to receive bits for these comparisons from circuitry on the circuit board 5 (*e.g.*, the deserializer 90 and the second BS generator 100).

[039] Finally, the controller 130 also preferably includes logic to maintain, increment, and clear a clock count 141, which indicates the number of clock cycles that occur during, for example, a measurement of the turn-on or turn-off time of the DUT 170. The controller 130 also preferably includes logic for storing measurement data 142. The substance and use of the clock count 141 and the measurement data 142 is described in more detail below.

[040] The clock source 145 is designed to provide a clock signal at a desired frequency. The clock source 145 may comprise a single, self-contained circuit (e.g., a Amptron® or Cardinal Components, Inc. crystal based oscillator). Such circuits are preferably single frequency circuits, but the clock source 145 may also have multiple-

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frequency capability. The clock source 145 may also comprise a plurality of circuits including a primary circuit and external timing components.

[041] Preferably, the clock source 145 includes a plurality of ports to communicate a clock signal to some or all of the circuitry and devices illustrated in Figure 1 (ports and connections not illustrated). The clock source 145 preferably includes an I/O port to receive configuration data from the controller 130 (*e.g.*, a desired frequency) (ports and connection not illustrated). Also not illustrated in Figure 1 are one or more demultiplexers and/or one or more dividers or multipliers that may be used to enable the clock source 145 to drive two or more components at one or more frequencies. For example, the SERDES 20, programmable delay 30, and deserializer 90 typically operate at a higher frequency than the controller 130 and the BS generators 10, 100.

[042] The DUT 170 and the master device 180 are preferably any electronic device capable of receiving, transforming, and transmitting a data signal. Typically, these devices are optoelectronic transceivers. As such, these devices are capable of receiving a data signal in an electrical form and transmitting the data signal in an optical form and vice versa.

[043] Each of these devices preferably include a D_{in} and D_{out} port (*e.g.*, the D_{in} port 172 and D_{out} port 174 and the D_{in} port 186 and D_{out} port 188 of the DUT 170 and the master device 180, respectively) and an I/O port (*e.g.*, the I/O port 179 and the I/O port 189 of the DUT 170 and the master device 180, respectively).

[044] The D_{in} port 172 of the DUT 170 is configured to receive data electrically from the SERDES 20. The D_{out} port 174 of the DUT 170 is configured to transmit data optically to the master device 180. The D_{in} port 186 of the master device 180 is

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configured to receive data optically from the DUT 170. The D_{out} port 188 of the master device 180 is configured to transmit data electrically to the programmable delay 30.

[045] The I/O ports are used to exchange control signals with the controller 130. In particular, the DUT 170 (and the master device 180) may receive, for example, a Transmitter Disable signal from the controller 130. Depending on the state of this signal (*e.g.*, a digital one or zero), the optical transmitter circuitry of the DUT 170 is enabled or disabled. Finally, the master device 180 is preferably a device that has been confirmed to operate properly. The master device 180 provides the system 1 with the ability to receive a data stream of optical signals and convert that data stream into an electrical signal.

[046] Referring to Figure 2, there is shown a more detailed illustration of the computer 160. In addition to the I/O port 162 illustrated in Figure 1, the computer 160 preferably includes standard computer components such as one or more processing units 204, a user interface 206 (*e.g.*, keyboard, mouse, and a display), memory 208, and one or more busses 210 to interconnect these components. The memory 208, which typically includes high speed random access memory as well as non-volatile storage such as disk storage, may store an operating system 212, a control module 214, and a database (or one or more files) 216, which may include a plurality of records 218. The operating system 212 may include procedures for handling various basic system services and for performing hardware dependent tasks. The one or more processing units 204 may execute, for example, tasks for the control module 214 under the direction of the operating system 212. The operating system may also provide the control module 214 with access to other system resources such as the memory 208 and the user interface 206.

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[047] The control module 214 is designed to manipulate the system 1 in accordance with the present invention. In particular, the control module 214 preferably interacts with the controller 130 through the I/O port 162 to initiate and monitor measurements of the DUT 170. As described in more detail below, the control module 214 directs the controller 130 to initialize one or more other components included in the system 1 and, if need be, to obtain information about the one or more other components that are not connected directly to the computer 160. The control module 214 may engage in such communication with the controller 130 before, during, and after measurements of the DUT 170. The control module 214 may communicate results of DUT measurements through the user interface 206 as needed. Finally, the computer 160 may communicate with other devices, such as Digital Communication Analyzers (not illustrated), during measurements of a DUT 170. Persons skilled in the art recognize that a Digital Communication Analyzer can provide additional information about the operation of a DUT 170 by monitoring the data transmitted by the DUT 170.

[048] Although separate ports are illustrated in Figures 1 and 2 and discussed above with respect to various circuitry, some embodiments of the present invention may include additional or fewer ports without departing from the scope of the present invention. For example, a single data bus with address bits and corresponding ports may be substituted for some or all of the data ports and corresponding connections illustrated in Figure 1. Additionally, some or all of the port connections, though illustrated in Figures 1 and 2 as single leads, may be formed by a plurality of separate leads. The configuration illustrated in Figures 1 and 2, therefore, represents just one embodiment and is not meant to limit the scope of the present invention.

II. Determining the Turn-off/on-Time of a Transmitter

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[049] Referring to Figures 3A-3E, there are shown a series of processing steps included in a preferred embodiment of the present invention. The steps of Figures 3A-3E may be conceptually divided into five somewhat overlapping phases. In a first phase (*e.g.*, steps 302-304), the circuitry and devices illustrated in Figure 1 are initialized. In a second phase (*e.g.*, steps 310-340), the data received from the master device is properly aligned with a clock signal. In a third phase (*e.g.*, steps 341-358), a proper configuration of the system 1, the DUT 170, and the master device 180 is confirmed and a seed value used by the second BS generator during the fourth phase is identified. The third phase preferably continues until consecutive groups of bits without any bit errors are transmitted or until it times out. In a fourth phase (*e.g.*, steps 360-389), data needed to compute the turn-on and turn-off times of the DUT 170 is gathered. In a fifth phase (*e.g.*, steps 390-394), the turn-on and turn-off times are calculated for the DUT 170 and/or the results of the measurement (attempt) are displayed.

A. Phase I: Initializing the System

[050] In a first phase, the control module 214 initializes the system 1 (step 302, Figure 3A). In particular, the control module 214 preferably directs the controller 130 to set the clock frequency of the clock signal generated by the clock source 145 and to turn the clock source 145 on. The control module 214 may also direct the controller 130 to set the length, type, and other characteristics of bit sequences generated by the BS generators. The controller 130 accomplishes this task by, for example, transmitting control signals through its first I/O port 131 and second I/O port 133 to the I/O port 12 and the I/O port 102 of the first and second BS generators 10, 100, respectively. The control module 214 may also direct the controller 130 to clear the clock count 141 and

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the measurement data 142. The control module 214 may create a new record 218 in the database 216 to store results of a DUT 170 measurement. Finally, the control module preferably directs the controller 130 to set the delay value of the programmable delay 30. In preferred embodiments of the present invention, this delay value is initially set to the lowest delay value possible. As persons skilled in the art know, some programmable delay circuits have an inherent non-zero, minimum delay value.

[051] The control module 214 then initializes external devices (step 304). In particular, the control module 214 preferably directs the controller 130 to turn on the DUT 170 and the master device 180 and enable the optical transmitter circuitry of the DUT 170 by, for example, adjusting the state of a Transmitter Disable control signal. More specifically, the controller 130, under the direction of the control module 214, may transmit these control signals through its I/O port 139 to the I/O port 179 of the DUT 170 and through its I/O port 140 to the I/O port 189 of the master device 180.

[052] The control module 214 then initiates the generation of a sequence of bits (step 310). This task is preferably completed by the controller 130, under the direction of the control module 214. In particular, the controller 130 may transmit a seed value through its D_{out} port 132 to the D_{in} port 14 of the first BS generator 10. In some embodiments of the present invention, the controller 130, under the direction of the control module 214, also transmits a control signal through its I/O port 131 to the I/O port 12 of the first BS generator 10 to enable the generation of the sequence of bits by the BS generator 10.

B. Phase II: Synchronizing the Bit Sequence with the Clock

[053] In response to step 310, the first BS generator 10 begins generating a sequence of bits by generating a bit group in the sequence of bits (step 312). In

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preferred embodiments of the present invention, bit groups are generated sequentially and transmitted in parallel. The BS generator 10 preferably operates (*i.e.*, generates bit groups) at the frequency of a clock signal originating from the clock source 145 (connections not illustrated). The first BS generator 10 continues to generate bit groups in the sequence of bits (repeating the sequence of bits if necessary) until disabled by the controller 130.

[054] Each bit group generated by the first BS generator 10 is serialized by the SERDES 20 and transmitted to the DUT 170 (step 314). In other words, the SERDES 20 receives bit groups through its D_{in} port 22 from the first BS generator 10 in parallel, but transmits these bit groups serially through its D_{out} port 24.

[055] The DUT 170 receives bits transmitted by the SERDES 20 through its D_{in} port 172 in an electrical form and transmits them in an optical form through its D_{out} port 174 to the master device 180. The master device 180 receives bits transmitted by the DUT 170 through its D_{in} port 186 in an optical form and transmits them in an electrical form through its D_{out} port 188 to the deserializer 90 via the programmable delay 30.

[056] The programmable delay 30 separately receives bits transmitted by the master device 180 and delays by a specified amount before transmitting these bits to the deserializer 90 (step 316). More specifically, the programmable delay 30 receives bits transmitted serially by the master device 180 through its D_{in} port 32 and transmits these bits after the specified delay through its D_{out} port 34 to the deserializer 90.

[057] The deserializer 90 receives bits transmitted serially by the programmable delay 30 and parallelizes them (step 318). More specifically, the deserializer 90, using a clock signal from the clock source 145, receives bits transmitted serially by the programmable delay 30 through its D_{in} port 92 and transmits these bits as a bit group in

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parallel through its D_{out} port 94 to both the controller 130 and the second BS generator 100. The clock signal used by the deserializer to receive serial data bits may be the fastest clock generated by the clock source 145.

[058] The second BS generator 100 generates a subsequent bit group from the bit group received through its D_{in} port 104 from the deserializer 90 (step 320). Bit sequences generated by the BS generators illustrated in Figure 1 are deterministic, so when configured in the same manner, these BS generators generate the same bit group from a given bit group. The output of the first BS generator 10 is typically fed back to the first BS generator 10 to generate another bit group in the sequence of bits. Similarly, the second BS generator 100 uses the bit group transmitted to it by the deserializer 90 as a seed value to generate a subsequent bit group in the sequence of bits. Because the second BS generator 100 is configured to produce the same sequence of bits as the first BS generator 10, the second BS generator 100 generates the same bit group that the first BS generator 10 generates from a given bit group.

[059] The subsequent bit group is transmitted by the second BS generator 100 through its D_{out} port 106 to the second D_{in} port 137 of the controller 130, but the subsequent bit group is not output by the second BS generator 100 until a subsequent clock cycle. And while the deserializer 90 transmits the bit group to the BS generator 100 in step 318, the programmable delay 30 delays another bit group received from the master device 180 (step 324). The deserializer then parallelizes this bit group (step 326). As indicated above, parallelizing a bit group includes transmitting the bits in parallel to both the controller 130 and the second BS generator 100. So the bit group received in step 324 is transmitted to the controller 130 during the same clock cycle in

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which the subsequent bit group generated by the BS generator 100 in step 320 is transmitted to the controller 130.

[060] The controller 130 compares the bit groups transmitted by the deserializer 90 and the Second BS generator 100, respectively (step 328, Figure 3B). If there are any bit errors (*i.e.*, one or more of the bits do not match) (step 330- Yes), the results of the comparison (*e.g.*, the number of bit errors) along with the delay value of the programmable delay 30 are stored as part of the measurement data 142 (step 332).

[061] If there are no bit errors (step 330-No) or after storing the results of the comparison and the delay value (step 332), the controller 130 determines whether the delay value of the programmable delay 30 is equal to the delay value maximum (step 334). This determination can be made by, for example, interfacing with the programmable delay 30 through an I/O port or by maintaining the current delay value as part of the measurement data 142 and updating it each time the programmable delay 30 is updated. In some embodiments of the present invention, the delay value maximum is approximately equal to the duration of two unit intervals of the data signal transmitted through the DUT 170 and master device 180.

[062] If the delay value of the programmable delay 30 is not equal to the delay value maximum (step 334-No), the controller 130 computes a new delay value for the programmable delay 30 (336). The new delay value is preferably computed by incrementing the current delay value by an amount that is a fraction of the unit interval mentioned in the preceding paragraph. The controller 130 then sets the programmable delay 30 with the new delay value (step 337). The controller 130 may also update the measurement data 142 to include the new delay value as well.

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[063] Steps 320-337 are then preferably repeated until the delay value of the programmable delay 30 is equal to the delay value maximum (step 334-Yes). When this occurs, the controller 130 computes an ideal delay value from the bit error counts and corresponding delay values stored in the measurement data 142 (step 338).

[064] In one embodiment, the controller 130 begins by sequentially scanning the bit error counts and corresponding delay values stored in the measurement data 142 for a first delay, which corresponds to a bit error count below a defined threshold. The scanning preferably begins with the minimum delay and ends with the maximum delay. After locating the first delay, scanning continues for a second delay, which corresponds to a bit error count above the defined threshold. Bit error counts above the defined threshold tend to occur when a data signal is sampled at or close to a temporal boundary of a bit period since a data signal does not switch from one state to another instantaneously. The threshold is preferably selected, therefore, so that an equal or greater bit error count is indicative of a sample taken near a temporal boundary of a bit period instead of just bit errors that can and do occur for other reasons. Similarly, the threshold is preferably selected so that it is unlikely that the bit error count of subsequent delays will drop below the threshold until after a temporal boundary of the bit period has passed. This last requirement prevents small increases in bit error counts, which might not be associated with a temporal boundary of a bit period, from being misinterpreted.

[065] Additionally, the increment used to adjust the delay value in step 336 is preferably small enough so that at least one delay corresponds to the region of time at or just before a temporal boundary of a bit period and at least one delay corresponds to the region of time just after a temporal boundary of a bit period. As a result, the second

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delay ideally corresponds to the region of time at or just before a temporal boundary of a bit period.

[066] After finding the second delay, scanning continues for a third delay, which corresponds to a bit error count below the defined threshold. And ideally, the third delay corresponds to a region of time just after a temporal boundary of a bit period.

[067] After finding the second and third delays (*e.g.*, a first temporal boundary of a bit period), the controller 130 continues scanning for a fourth and fifth delay (*e.g.*, a second temporal boundary of the bit period). The fourth delay is the next delay corresponding to a bit error count above the defined threshold. Additionally, the fifth delay is the next delay - following the fourth delay - corresponding to a bit error count below the defined threshold.

[068] After the second, third, fourth, and fifth delays are located (*e.g.*, two temporal boundaries of a bit period have been located), they are summed and divided by four. The result is a delay value that corresponds to a sampling position roughly midway between the temporal boundaries of a bit period.

[069] Note that in some embodiments of the present invention, a plurality of bit groups are transmitted for each value of the delay value stored in the programmable delay 30. In these embodiments, the clock count 141 may be used to track how many bit groups have been transmitted with a given delay value. Each time the delay value is updated, the clock count 141 is cleared. In these embodiments, an extra test may be conducted before calculating and setting the delay value in steps 336 and 337. If some predefined count value has not yet been reached, steps 336 and 337 are not executed before returning to step 320. Transmitting a plurality of bit groups for each delay value enables a more accurate determination of the ideal delay value. Also, the clock count

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141 is cleared upon completion of this phase as well so as not to interfere with the next phase.

C. Phase III: Testing the System and Generating a Seed Value

[070] The controller 130 then sets the programmable delay 30 with the ideal delay value calculated in step 338 (step 340) and begins incrementing the clock count 141 (step 341) each time a bit group is received from the deserializer 90.

[071] The second BS generator 100 then generates a subsequent bit group from a bit group received through its D_{in} port 104 from the deserializer 90 (step 342, Figure 3C). The subsequent bit group is transmitted by the second BS generator 100 through its D_{out} port 106 to the second D_{in} port 137 of the controller 130, but the subsequent bit group is not output by the second BS generator 100 until a subsequent clock cycle. And while the deserializer 90 transmits the bit group to the BS generator 100 in step 318, the programmable delay 30 delays another bit group received from the master device 180 (step 344). The deserializer then parallelizes this bit group (step 346) as described above.

[072] The controller 130 compares the bit groups transmitted by the deserializer 90 and the second BS generator 100, respectively (step 348) and stores the results of the comparison (*e.g.*, the number of bit errors) as part of the measurement data 142 (step 350).

[073] If there are any bit errors *(i.e.*, one or more of the bits do not match) (step 352- Yes), the controller 130, checks the value of the clock count 141 to determine whether it is greater than a predefined counter value (e.g., a counter value maximum) (step 354), which may be maintained by either the controller 130 or the computer 160.

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[074] As noted above, the purpose of the third phase is to confirm the configuration of the system 1, the DUT 170, and the master device 180 and to identify a seed value for the second BS generator 100. If the clock count 141 exceeds the predefined counter value, it may be safely assumed that the system 1, the DUT 170, and the master device 180 are not configured properly.

[075] If the clock count 141 is not greater than the predefined counter value (step 354-No), the controller 130, under the direction of the control module 214, may clear the bit error count stored in the previous execution of step 350 (step 356). The cycle of receiving bit groups, generating subsequent bits groups, and comparing the two then continues until there are no bit errors or the clock count 141 exceeds the predefined counter value. Note that the second BS generator 100 continues to accept new bit sequence seed values from the deserializer 90. Because there were one or more bit errors detected during the most recent bit group comparisons, it may be that the bit sequence seed values used to produce two of the compared bit groups are invalid.

[076] If the clock count 141 is greater than the predefined counter value (step 354-Yes), the results of the measurement may be displayed via the user interface 206 (step 394). If step 394 is reached in this fashion, the results will indicate that there is a problem with the configuration of the DUT 170, the master device 180, and/or the system 1 and that an actual measurement was never made.

[077] Returning to step 352, if there are no bit errors (step 352-No), the controller 130, under the direction of the control module 214, clears the clock count 141 (step 357), directs the second BS generator 100 to stop accepting bit groups from the deserializer 90 (step 358), and disables the optical transmitter circuitry of the DUT 170 (step 360, Figure 3D).

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D. Phase IV: Collecting Transmitter Data and Calculating the Turn-off and Turn-on Time

[078] Step 358 marks the end of the third phase and the beginning of the fourth phase. As indicated above, the third phase identifies a bit sequence seed value for the second BS generator 100. This happens when consecutive bit group are transmitted without bit errors. This means that the second BS generator 100 may now generate the exact bit sequence generated by the first BS generator 10 without additional bit sequence seed values from the deserializer 90. Instead, the subsequent bit groups generated by the second BS generator 100 will now be fed back to the second BS generator, as seed values to generate additional subsequent bit groups. The controller 130 may direct the second BS generator 100 to stop accepting bit groups from the deserializer 90 by, for example, transmitting control signals through its second I/O port 133 to the I/O port 102 of the second BS generators 100. Further, the controller 130 may disable the optical transmitter circuitry of the DUT 170 by, for example, adjusting the state of a Transmitter Disable signal transmitted to the DUT 170 through the fifth I/O port 139 of the controller 130 and the I/O port 179 of the DUT 170.

[079] The second BS generator 100 then generates a subsequent bit group from the "subsequent bit group" compared during the most recent execution of step 348 (step 362). This previous "subsequent bit group" is fed back to the second BS generator 100. The programmable delay 30 delays another bit group received from the master device 180 (step 364) and then the deserializer 90 parallelizes this bit group (step 366) as described above.

[080] The controller 130 then compares the bit groups transmitted by the deserializer 90 and the second BS generator 100, respectively (step 368). If there are

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not any bit errors (step 370 No), steps 362-368 are repeated. But if there are any bit errors (step 370- Yes), the controller 130 stores the bit group received from the deserializer 90 and the value of the clock count 141 as part of the measurement data 142 (steps 372).

[081] Further, if all of the bits are not digital zeroes (step 373-No), steps 362-368 are repeated. In other words, the controller 130 continues to store bit groups and values of the clock count 141 in step 372 until the DUT 170 is completely off (*i.e.*, when all of the bits "output" by the DUT 170 are digital zeroes). Storing these bit groups enables the calculation of a turn-off time with unit interval precision as described in more detail below.

[082] Once all of the bits are digital zeroes (step 373-Yes), the controller waits a predefined period of time and then clears the clock count 141 (step 374) and enables the optical transmitter circuitry of the DUT 170 (step 376). The amount of time waited by the controller 130 may change from one embodiment to the next. The clock count 141 is cleared so that a subsequent count corresponds to clock cycles that occur after the optical transmitter circuitry of the DUT 170 is enabled in step 376. Further, the controller 130 may enable the optical transmitter circuitry of the DUT 170 by, for example, readjusting the state of a Transmitter Disable signal transmitted to the DUT 170.

[083] The second BS generator 100 then generates a subsequent bit group from the "subsequent bit group" compared during the most recent execution of step 362 (step 378, Figure 3E). This previous "subsequent bit group" is fed back to the second BS generator 100. The programmable delay 30 delays another bit group received from the

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master device 180 (step 380) and then the deserializer 90 parallelizes this bit group (step 382) as described above.

[084] The controller 130 then compares the bit groups transmitted by the deserializer 90 and the second BS generator 100, respectively (step 384). If all of the bits are in error (step 386- Yes), steps 378-384 are repeated. But if not all of the bits are in error (step 386-No), the controller 130 stores the results of each bit comparison and the value of the clock count 141 as part of the measurement data 142 (step 388). And if there are any bits in error (step 389- Yes), steps 378-384 are repeated. In other words, the controller 130 continues to store results of bit comparisons (and corresponding values of the clock count 141) until there are no bit errors.

[085] Once there are no bit errors (step 389-No), the controller 130 calculates the turn-off and turn-on times of the DUT 170 from the data stored in steps 372 and 388, respectively (step 390). In some embodiments, the controller 130 transmits the data stored in steps 372 and 388 to the computer 160, which then calculates the turn-off and turn-on times of the DUT 170. In other embodiments, the controller 130 calculates the turn-off and turn-on times of the DUT 170 and then transmits the results to the computer 160.

[086] In preferred embodiments, computing the turn-off time includes scanning in reverse order from the end of the last bit group stored in step 372 for the bit position of the "last bit" in a string of bits equal to a digital zero and identifies, as the "last clock count value," the value of the clock count 141 that corresponds to the bit group in which this last bit is included. Also, the controller 130 or the computer 160 makes use of a known delay value of the optical fiber ("optical fiber delay") connecting the DUT 170 to the master device 180. This information is then input to an equation as follows:

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((((LAST CLOCK COUNT VALUE - 1) * (NUMBER OF BITS IN A BIT GROUP)) + (BIT POSITION OF THE LAST BIT - 1)) / (BIT RATE OF THE BITS TRANSMITTED SERIALLY)) - (OPTICAL FIBER DELAY).

[087] In preferred embodiments, computing the turn-on time includes scanning in reverse order from the end of the penultimate bit group stored in step 388 for the bit position of the "last bit" in a string of bits not in error and identifies, as the "last clock count value," the value of the clock count 141 that corresponds to the bit group in which this last bit is included. This information is then input to an equation as follows:

((((LAST CLOCK COUNT VALUE - 1) * (NUMBER OF BITS IN A BIT GROUP)) + (BIT POSITION OF THE LAST BIT - 1)) / (BIT RATE OF THE BITS TRANSMITTED SERIALLY)) - (OPTICAL FIBER DELAY).

[088] The computer 160 may then store the results of the measurement in a record 218 of the database 216 (step 392) and display the results of the measurement via the user interface 206 (step 394). If step 394 is reached in this fashion, the results include the turn-off and turn-on times calculated in step 390.

[089] The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. For example, the steps illustrated in Figures 3A-3E have been described as occurring sequentially. Some of these steps, however, may actually occur at roughly the same time or in parallel (*e.g.*, steps 360 and 362 and steps 378 and 380, respectively). The described embodiments are to be considered in all respects only as illustrative and not restrictive. The scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing

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description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

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